**In order to achieve the assessment criteria (P8) you must answer the following task:**

**Task 1**

Compare between TTL and CMOS Logic families in terms of:

* Technology used.
* Power consumption.
* Speed.
* Two input **NOR** gate implementation.
* Voltage levels.

 **(P8)**

**In order to achieve the assessment criteria (P9) you must answer the following task:**

**Task 2**

Design and Construct the following combinational logic circuits:

* NAND gate using NOR gates only.
* Landing Gear Warning Circuit shown in Fig(1) ( Note: you have only NAND gates)



Fig (1)

**(P9)**

**In order to achieve the assessment criteria (P10) you must answer the following task:**

**Task 3**

Evaluate the following digital electronic circuit in terms of:

* Function.
* Operation.
* Timing diagram.

Fig (2)

 **(P10)**